What is Claimed is:

1. A method of making a printed wiring board, comprising:

forming a first innerlayer panel, wherein forming the first innerlayer panel comprises:

forming a first electrode layer comprising a plurality of electrode portions;

forming a dielectric contacting the first electrode layer;

forming a second electrode layer spaced from the first electrode layer, wherein the first electrode layer, the dielectric and the second electrode layer form a first capacitor;

connecting the first capacitor to an organic dielectric material; and

trimming at least a part of at least one of the electrode portions; and

connecting the first innerlayer panel to at least one additional innerlayer panel.

2. The method of claim 1, wherein trimming comprises:

trimming one or more electrode portions with a laser.

3. The method of claim 2, wherein:

the laser strikes a trimmed electrode portion with a laser beam at a point that does not overlie a portion of the second electrode layer.

4. The method of any one of claims 2 or 3 wherein the laser is programmed with an electrode design and utilizes a feedback process in which the laser initially measures total capacitance and calculates the number of electrode portions that are required to be trimmed.

5. The method of claim 4 wherein the laser measures the capacitance throughout trimming.

6. The method of claim 5 wherein the laser is programmed to stop trimming within a specified range of the desired capacitance value.

7. The method of any one of claims 1-6, wherein connecting the first capacitor to an organic dielectric material comprises:

substantially encasing the first capacitor within organic dielectric material.

8. The method of any one of claims 1-7, wherein forming the first electrode layer comprises:

forming a main electrode portion of larger size than the plurality of electrode portions.

9. The method of any one of claims 1-8, wherein forming the second electrode layer comprises:

forming a plurality of second electrode portions, wherein the second electrode portions are interdigitated with the electrode portions of the first layer.

10. The method of any one of claims 1-9, wherein the thickness of the electrode layers is in the range of 10-50 microns.

11. The method of any one of claims 1-10, wherein forming the second electrode layer comprises:

providing a metallic foil; and

etching the foil.

12. The method of any one of claims 1-11, wherein connecting the first innerlayer panel to at least one additional innerlayer panel comprises:

laminating the first innerlayer panel to an additional innerlayer panel.

13. A capacitor, comprising:

a first electrode comprising a first plurality of electrode portions;

a second electrode comprising a second plurality of electrode portions spaced from the first plurality of electrode portions; and

a dielectric contacting the first electrode portions.

14. The capacitor of claim 13, further comprising:

a dielectric material that contacts and substantially encases the capacitor.

15. The capacitor of any one of claims 13 or 14 wherein one or more of the first plurality of electrode portions are trimmed to achieve a target capacitance value.

16. A capacitor, comprising:

a first electrode comprising a first plurality of electrode portions;

a second electrode comprising a second plurality of electrode portions spaced from and interdigitated with the first plurality of electrode portions; and

a dielectric disposed between the first and second pluralities of electrode portions.

17. The capacitor of claim 16, further comprising:

a dielectric material that contacts and substantially encases the capacitor.

18. The capacitor of any one of claims 16 or 17 wherein one or more of the first plurality of electrode portions are trimmed to achieve a target capacitance value.

19. The capacitor of any one of claims 13-18, wherein:

the first plurality of electrode portions comprises at least four electrode portions.

20. A printed wiring board formed by the method of any one of claims 1-12.

21. A printed wiring board containing the capacitor of any one of claims 13-18.